



Claim 29 (Currently amended): ~~The~~ A circuit arrangement according to ~~Claim 24~~, wherein the switching transistors are connected such that, in an operating state of the circuit arrangement in which at least one supply voltage of the circuit arrangement is switched off, comprising:

a flip-flop having a plurality of storage transistors with a threshold voltage of a first value;

a first power switch transistor having a threshold voltage of a second value, wherein an application of a predetermined electrical potential to the first power switch transistor's gate terminal brings the circuit arrangement to an operating state in which if at least one supply voltage is switched off, electric charge carriers contained in the circuit arrangement are prevented from discharging from the circuit arrangement;

a plurality of switching transistors, having a threshold voltage of a third value, provided between the flip-flop and the first power switch transistor, for coupling a flip-flop input signal into the flip-flop wherein at least one ~~each~~ of the terminals of the switching transistors has a defined electrical potential in the operating state; and

wherein the magnitude of the first and/or the second value is greater than the magnitude of the third value.

Claim 30 (Currently amended): The circuit arrangement according to Claim ~~24~~ 29, having at least one second power switch transistor, which is coupled to at least a portion of the switching transistors such that, in an operating state of the circuit arrangement in which at least one supply voltage of the circuit arrangement is switched off, a gate terminal of each of the switching transistors coupled to the at least one second power switch transistor has a defined electrical potential.



Claim 35 (Previously presented): The circuit arrangement according to Claim 33, wherein the pulse generator circuit comprises a logic subcircuit that generates at least one flip-flop input signal from at least one input signal in accordance with a predetermined logic operation.

Claim 36 (Previously presented): The circuit arrangement according to Claim 35, wherein the logic subcircuit operates as one of an inverter, AND gate, OR gate, NAND gate, NOR gate, exclusive OR gate, and exclusive NOR gate.

Claim 37 (Currently Amended): The circuit arrangement according to Claim 36, wherein the logic subcircuit comprises a plurality of logic transistors having a threshold voltage of a ~~fifth~~ fourth value, wherein the magnitude of the first and/or the second value is greater than the magnitude of the ~~fifth~~ fourth value.

Claim 38 (Cancelled)

Claim 39 (Currently Amended): The circuit arrangement according to Claim 24 37, further comprising a test circuit coupled to the flip-flop, wherein the test circuit tests functionality of the flip-flop.

Claim 40 (Previously presented): The circuit arrangement according to Claim 39, wherein the test circuit has an input component that programs a test input signal of the flip-flop, and an output component that reads a test output signal of the flip-flop.

Claim 41 (Currently Amended): The circuit arrangement according to Claim 39, wherein the test circuit has a plurality of test transistors with a threshold voltage having a ~~sixth~~ fifth value, wherein the magnitude of the ~~sixth~~ fifth value is greater than at least one of the magnitudes of the third to ~~fifth~~ fourth values.

Claim 42 (Previously presented): The circuit arrangement according to Claim 41, wherein the test transistors have a gate insulating layer having a thickness greater than a thickness of the gate insulating layer of the switching transistors.

Claim 43 (Currently Amended): The circuit arrangement according to Claim 34 41, wherein the test transistors have a gate insulating layer having a thickness greater than a thickness of a gate insulating layer of the pulse generator transistors.

Claim 44 (Currently Amended): The circuit arrangement according to Claim 37 41, wherein the test transistors have a gate insulating layer having a thickness greater than a thickness of a gate insulating layer of the logic transistors.



couple or decouple the flip-flop and the switching transistors, and the magnitude of the ~~seventh~~ fifth value is greater than the magnitude of the third value, and

wherein the protection transistors have a gate insulating layer having a thickness greater than the thickness of a gate insulating layer of the logic transistors.

Claim 49 (Previously presented): The circuit arrangement according to Claim 45, wherein

in a first operating state, when at least one supply voltage of the circuit arrangement is switched off, by applying electrical control signals to at least a portion of the protection transistors, the protection transistors electrically decouple the flip-flop and the switching transistors from one another; and

in a second operating state, when supply voltages are applied to the circuit arrangement, by applying electrical control signals to at least a portion of the switching transistors, the switching transistors electrically couple the flip-flop and the switching transistors to one another.

Claim 50 (Previously presented): The circuit arrangement according to Claim 45, wherein the protection transistors have at least one transistor pair of transistors of different conduction types connected in parallel with one another, and at least one transistor pair connected by its source/drain terminals between the flip-flop and the switching transistors.

Claim 51 (New): A circuit arrangement comprising:

a flip-flop having a plurality of storage transistors with a threshold voltage of a first value;

